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TITLE: Semiconductor device forming an insulating
layer buried
on the SOI substrate

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PATENT-ASSIGNEE: FUJITSU LTD[FUIT]

PRIORITY-DATA: 2000WO-JP01435 (March 9, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE
PAGES MAIN-IPC		
US 7005755 B2	February 28, 2006	N/A
000 H01L 023/544		
WO 200167509 A1	September 13, 2001	J
051 H01L 021/70		
US 20030008472 A1	January 9, 2003	N/A
000 H01L 021/76		
KR 2002077936 A	October 14, 2002	N/A
000 H01L 021/027		
JP 2001566184 X	September 16, 2003	N/A
000 H01L 021/027		
US 6706610 B2	March 16, 2004	N/A
000 H01L 021/76		
US 20040135226 A1	July 15, 2004	N/A
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DESIGNATED-STATES: JP KR US

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO
APPL-DATE		
US 7005755B2	Cont of	2000WO-JP01435
March 9, 2000		
US 7005755B2	Div ex	2002US-0231046
August 30, 2002		
US 7005755B2	N/A	2003US-0745645
December 29, 2003		
US 7005755B2	Div ex	US 6706610
N/A		
WO 200167509A1	N/A	2000WO-JP01435

March 9, 2000		
US20030008472A1	Cont of	2000WO-JP01435
March 9, 2000		
US20030008472A1	N/A	2002US-0231046
August 30, 2002		
KR2002077936A	N/A	2000WO-JP01435
March 9, 2000		
KR2002077936A	N/A	2002KR-0711701
September 6, 2002		
JP2001566184X	N/A	2000WO-JP01435
March 9, 2000		
JP2001566184X	N/A	2001JP-0566184
March 9, 2000		
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N/A		
US 6706610B2	Cont of	2000WO-JP01435
March 9, 2000		
US 6706610B2	N/A	2002US-0231046
August 30, 2002		
US20040135226A1	Cont of	2000WO-JP01435
March 9, 2000		
US20040135226A1	Div ex	2002US-0231046
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US20040135226A1	N/A	2003US-0745645
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US20040135226A1	Div ex	US 6706610
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ABSTRACTED-PUB-NO: WO 200167509A

BASIC-ABSTRACT:

NOVELTY - A semiconductor device formed on a SOI substrate includes isolation trenches formed in a first region and reaching an insulating layer buried in the SOI substrate, and alignment marks formed in a second region and consisting of grooves extending into a support substrate.

USE - Semiconductor device forming an insulating layer buried on the SOI substrate

CHOSEN-DRAWING: Dwg.2D/7

TITLE-TERMS: SEMICONDUCTOR DEVICE FORMING INSULATE LAYER BURY SOI
SUBSTRATE

DERWENT-CLASS: P84 U11

EPI-CODES: U11-C08A3;

SECONDARY-ACC-NO:

Non-CPI Secondary Accession Numbers: N2002-184828